

Amendments to the Claims:

Please amend claims 1 and 26.

The listing of claims that follows will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of testing a semiconductor device ~~having a memory,~~
comprising:

selecting a portion of said a memory, said memory comprised by said semiconductor
device;

testing said selected portion of said memory;

designating said selected portion of said memory as a designated memory in response to
an acceptable testing result; and

storing data in said designated portion of said memory for retrieval at a later time, said
data comprising test data resultant from additional testing of said semiconductor device and
unrelated to testing said selected portion of said memory.

2. (Original) The method of claim 1, further including attempting a soft repair of said selected
memory portion in response to an unacceptable test result and designating said selected portion
of memory in response to a successful repair.

3. (Original) The method of claim 2, further including selecting and testing additional memory portions of said memory in response to an unacceptable test result and unsuccessful repair attempt until a portion of said memory having an acceptable test result or successful repair is found.
4. (Original) The method of claim 1, wherein said selected portion of memory is selected to have a sufficient word length and number of bits for storing said data.
5. (Original) The method of claim 1, further including compressing said data before storing said data in said designated portion of said memory.
6. (Original) The method of claim 5, further including decompressing said data after retrieving said data from said designated portion of said memory.
7. (Original) The method of claim 1, wherein said data comprises bitmaps, memory fail data, LBIST patterns or pass/fail data.
8. (Original) The method of claim 1, further including sending said data to a tester.
9. (Original) The method of claim 1, wherein said data is generated by ABIST or LBIST.
10. (Original) A method of testing a semiconductor device having a memory, comprising:
providing a designated memory;

performing ABIST on a memory segment to generate memory test data;
storing said memory test data in said designated memory; and
retrieving said test data at a later time.

11. (Original) The method of claim 10, wherein said memory test data is a bitmap.

12. (Original) The method of claim 10, wherein said memory test data is fail data generated from a bitmap.

13. (Original) The method of claim 12, further including ORing additional test data with said test data already stored in said designated memory.

14. (Original) The method of claim 10, further including compressing said data before storing said data in said designated memory.

15. (Original) The method of claim 14, further including decompressing said data after retrieving said data from said designated memory.

16. (Original) A method of testing a semiconductor device having a memory, comprising:

providing a designated memory;

performing an LBIST on a device logic function to generate a set of LBIST signatures;

storing said LBIST signatures in said designated memory; and

retrieving said LBIST signatures at a later time.

17. (Original) The method of claim 16, further including compressing said data before storing said data in said designated memory.

18. (Original) The method of claim 17, further including decompressing said data after retrieving said data from said designated memory.

19. (Original) The method of claim 16, wherein said LBIST is run on every group of N patterns, each group of N patterns having a cumulative fail signature.

20. (Original) The method of claim 19, further including :

identifying a failing group of N patterns;

performing a second LBIST on said device logic functions using every LBIST pattern from said group of N patterns; and

identifying every failing pattern in said group of N patterns.

21. (Original) A method of testing a function of a semiconductor device having a memory, comprising:

providing a designated memory;

performing a first test using a test pattern in a first corner of the test specification of said function of said semiconductor device;

storing the result of said first test in said designated memory;

performing a second test using said test pattern in a second corner of the test specification of said function of said semiconductor device;

retrieving said first test result from said designated memory; and

comparing said first test result with said second test result.

22. (Original) The method of claim 21, further including generating a pass signal in response to said first test result matching said second test result and generating a fail signal in response to said first test result not matching said second test result.

23. (Original) The method of claim 21 further including compressing said first test result before storing said first test result in said designated memory and decompressing said first test result after retrieving said first test result from said designated memory but before comparing said first test result to said second test result.

24. (Original) The method of claim 21 wherein said designated memory contains at least as many bits as there are latches in said function of said semiconductor device.

25. (Original) The method of claim 24, wherein said designated memory has a word length equal to the number of scan chains in said function of said semiconductor device.

26. (Currently Amended) A semiconductor device comprising:

a memory;

an ABIST engine adapted to test said memory; and

an interface adapted to send test data to and receive test data from a designated portion of said memory, said test data comprising data unrelated to testing said memory.

27. (Original) The semiconductor device of claim 26, wherein said interface is an ABIST interface and said test data is bitmap data.

28. (Original) The semiconductor device of claim 27, wherein said ABIST interface includes a data compress function and said ABIST engine includes a data decompress function.

29. (Original) The semiconductor device of claim 26, further including an LBIST engine adapted to test device logic functions and wherein said interface is an LBIST interface and said test data comprises test patterns.

30. (Original) The semiconductor device of claim 29, wherein said LBIST interface includes a data compress function and said LBIST engine includes a data decompress function.

31. (Original) The semiconductor device of claim 26, further including a corner compare function adapted to compare the results of a test pattern run in two corners of the test specification of said semiconductor device and wherein said interface is a corner interface and said test data is the result of a first corner test.

32. (Original) The semiconductor device of claim 31, wherein said corner interface includes a data compress function and said corner compare includes a data decompress function.

33. (Original) The semiconductor device of claim 26, further including a repair function adapted to soft repair said designated portion of said memory segment.